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10/821,935	04/12/2004	Kenji Tahara	HITA.0541	2141

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EXAMINER	
LE, DINH THANH	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,935	TAHARA ET AL	
	Examiner	Art Unit	
	DINH T. LE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objection

Claims 1 and 4-5 are objected to because the preamble and the body are not clearly recited. Correction is required.

Claim Rejections

Claim Rejections - 35 USC § 112

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required. For example,

In claim 1, the recitation "which bias voltages" on line 6 and "the transistors" on line 13 lacks clear antecedent basis. It is not understood what the "power voltages" of transistors on line 5 are, how the voltages can be "controlled" since no means for performing the controlling function is recited in the claim, how the gate terminals on line 6 can be "amplified", how the power voltage on line 12 can be "generated", where the "drain currents" on line 16 comes from, and how the recitation "differential transistors" on line 8 is read on the preferred embodiment or

seen on the drawings. The description of the present invention is incomplete because the amplifier circuit does not have an input/output. Thus, the claimed amplifier circuit may not perform the recited function. The same is true for claims 4-5 and 11.

In claim 2, the recitation "the transistors" on lines 3 and 13 lacks clear antecedent basis. It is unclear where "two voltages" on line 6 come from, if the recitation "one voltage" on line 7 "output power" on line 7, and "transistor" and "last stage" on line 11 are additional "voltage", "power", "transistor" and "last stage" or further recitation of the previously claimed "voltages" on line 5, "transistor" on line 4 of claim 2, "power" on line 4 and "last stage" on line 9 of claim 1. The same is true for reciting "control voltage" on line 3 and "output power" on line 4 of claim 3,

In claim 4, it is unclear how the recitation "dual-gate field effect transistor" is read on the preferred embodiment. Insofar as understood, no such transistor is seen on the drawings.

In claim 9, it is not understood what the "element" on line 4 is and how it is read on the preferred embodiment or seen on the drawings.

Claims 1-13 include unclear recitations and antecedent basis problems that makes the claims difficult to understand and follow as discussed above. Theses claims should be clarified and corrected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

> such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5, 7 and 9-10 are rejected under 35 USC 103 (a) as being unpatentable over Epperson et al (US 6,701,138) in view of Nakanishi et al (US 5,126,688).

As the best construed, Nakanishi et al discloses in Figures 1-2 and 7 a power amplifier comprising:

- three amplifier stages (60, 62, 64) in cascaded;
- variable voltage source (46) having a differential amplifier (68) and a voltage regulator such as a transistor (70) coupled to the transistors (62, 64) for providing variable voltages to the stages (62, 64); and
- a bias network (94)`for biasing the stages (60, 62, 64).

However, Epperson does not disclose that the stages are the FETS and the drain current of the preceding transistor is saturated in a state of lower control voltage than the last-stage transistor.

Nakanishi et al discloses in Figures 1-2 and 7 a power transistor circuit comprising FET transistors (Figure 7) for reducing power consumption and suggests separating controllable voltage sources (58,62, 64) for each transistor stages (32-34) so that each controllable voltage source provides adjustable power supply voltage for a respective amplifier stage for the purpose of independently controlling the amplifier stages that would stabilize the circuit with high power efficiency in a wide adjustable range and eliminate the nonlinearity of the characteristic between the output power and the feedback voltage, see lines 60-68, column 3 and lines 1-6, column 4.

It would have been obvious to a person having skill in the art at the time the invention was made to employ the FET transistors and separate control supply voltages of Epperson et al

suggested by Nakanishi et al for the purpose of reducing the power consumption and independently controlling the amplifier stages that would stabilize the amplifier circuit with high power efficiency in a wide operational range and eliminate the nonlinearity of the characteristic between the output power and the feedback voltage.

Also, a skilled artisan realizes that the overall output power of the power amplifier is a sum of a individual power provided by each amplifier stage which is determined by the size of the transistor. Since the size of the transistors are selectable, selecting the transistor size for the circuit of Epperson et al for providing a predetermined overall output power as recited in the claims is considered to be a matter of a design expedient for an engineer depending upon a particular environment and the application in which the modified amplifier of Epperson et al is to be used. Lacking of showing any criticality, it would have been obvious to a person having skill in the art at the time the invention was made to select the transistor size to have saturated drain currents as claimed for the purpose of providing a predetermined output power.

Claim 11 is rejected under 35 USC 103 (a) as being unpatentable over Sakumo (US 6,806,774) in view of Epperson et al (US 6,701,138) and further in view of Nakanishi et al (US 5,126,688).

Sakumo discloses in Figure 1 a circuit comprising:

- a baseband circuit (1011);
- a modulation/demodulation circuit (1009); and
- an adjustable amplifier (1002).

However, Nakanishi does not disclose that amplifier (1002) having a structure as claimed in claim1. Epperson et al in view of Nakanishi et al suggests an adjustable amplifier as stated above for preventing switching transients during changing bias and gain, see lines 40-49, column 2. It would have been obvious to a person having skill in the art at the time the invention was made to employ the modified amplifier circuit of Epperson et al in the circuit of Sakumo for the purpose of preventing switching transients during changing gain and bias.

Allowable Subject Matter

Claims 4, 6, 8 and 12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The claim is allowed because the prior art of record does not show the dual gate transistor as combined in claim 4, and the first amplifier and the second amplifier as combined in claim 12.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DINH LE
Primary Examiner